

ABSTRACT OF THE DISCLOSURE

**METHOD AND SYSTEM FOR CLOCK/DATA RECOVERY FOR
5 SELF-CLOCKED HIGH SPEED INTERCONNECT**

A method and system is provided for clock/data recovery for self-clocked high speed interconnects. A data signal is received and then equalized. The equalized data signal then 10 provides the trigger to separate "ones" and "zeros" one-shots. The equalized Manchester data signal is also integrated, compared with a threshold value to determine the negative and positive peaks of the data signal. Then after the appropriate peak is determined, a mid-bit signal is sent 15 as input to a set-reset flip-flop which thereby outputs an asynchronous recovered non-return to zero signal. This asynchronous recovered non-return to zero signal then provides an enable input to the "ones" one-shot and the complementary asynchronous recovered non-return to zero 20 signal provides an enable input to the "zeros" one-shot. The "ones" one-shot outputs a "ones" clock signal and the "zeros" one-shot outputs a "zeros" clock signal. These two signals are verified and a recovered clock out signal is provided. The asynchronous recovered non-return to zero 25 signal is supplied to a data flip-flop along with the recovered clock out signal and a constant and the result is a synchronous recovered non-return to zero signal.